REMARKS

Applicant thanks the Examiner for the thoughtful review of the application. The status of the claims is as follows: **Claims 1 - 2, Claims** and **4 – 48** are **Pending** in the present application. **Claims 1, 8, 9, 25, 33, 35,** and **44** have been **Amended** herein. Amendments to the claims are described below in the **PRESENT AMENDMENT**.

a. The Applicant respectfully request that the **Attorney Docket No.** for the present application be changed to **P030.04.CIP24+** as set forth on **Page 1** of a **Supplemental Application Data Sheet** submitted with the **RCE** filed on **09 August 2005.**

I. PRESENT AMENDMENT

Independent **Claims 1, 25, 33** and **44** were amended herein to particularly point out and distinctly claim the subject matter the Applicant regards as the invention. Specifically, those claims were amended to recite that the memory array is "a two-terminal cross point memory array" and that each memory cell in the array is a "two-terminal memory cell."

Support for the amendments can at least be found in the **Specification** as originally filed. For example, in **FIGS. 1A, 1B, 2A, 2B,** and **4** of the **Drawings** and in **Paragraphs 0016 – 0020** and **0022 – 0024** of the **Detailed Description.**

Claims 8, 9, and **35** were amended to correct typographical errors.

No new matter was introduced in amending the claims.

ii. **ARGUMENT**

a. **Rejection of Claims 1- 2 and Claims 4 - 48 under 35 U.S.C. §112 second paragraph**

The Applicant respectfully traverse the rejections of **Claims 1- 2 and Claims 4 - 48** under **35 U.S.C. §112** second paragraph. First, the Applicant notes that in the prior two office actions on the merits, mailed on 12/16/2004 and 06/09/2005 respectively, the Examiner did not raise any objections or rejections to the terms "high temperature", "stable", "not stable", or "fabrication greater than 450 °C" as being indefinite under **35 U.S.C. §112** second paragraph. It is only in the present office action, after the filing of the **RCE**, that Examiner contends that those terms are indefinite.

Second, one skilled in the microelectronics art understands the meaning of high temperature in regards to an allowable range of process temperatures that may be used in the fabrication of a microelectronic device. Moreover, one skilled in the microelectronics art understands that the allowable range of temperatures will depend on the materials present in the device under fabrication at the time the high temperatures are applied. The Examiner contends that the present application does not clearly define "high temperature" and the claims do not make clear "*how high is high.*" The Applicant respectfully submits that the **Detailed Description** clearly defines what is meant by "high temperature" in **Paragraphs 0038** through **0044**, under the heading of "High Temperature Fabrication."

For example, in **Paragraph 0038**, one skilled in the art understands that refractory metals have a high melting point and can be used in conjunction with layers of materials in a device that require high temperature processing (e.g., pulsed laser deposition, MOCVD, high temperature anneal). Therefore, if it is necessary to make a metal interconnect to one or more layers of material during processing at a high temperature, then the use of refractory metals that can withstand the high temperatures is the logical choice. Conversely, in **Paragraph 0039**, one skilled in the art understands that at the aforementioned high process temperatures, it would not be suitable to use low melting point metals such as aluminum (**Al**) and copper (**Cu**) because those metals

would lose their structural integrity, become damaged, or create defects due to diffusion of their atoms.

Accordingly, the terms "stable" and "not stable" are also clear and distinct to one skilled in the art because one skilled in the art possess the knowledge necessary to determine, based on the materials being processed, whether or not those materials will be stable or not stable at a given high temperature. In Paragraph **0040**, Applicant clearly states that a high temperature is typically between 600 °C and 800 °C to grow a crystalline or a polycrystalline structure for a multi-resistive state element. Therefore, based on a high temperature range typically between 600 °C and 800 °C, one skilled in the art can easily determine that refractory metals, as opposed to **Al** or **Cu**, are well suited for use within that range of high temperatures.

Third, as for **Claim 33**, the Examiner contends that "wherein the memory plugs have at least one layer that requires the minimum temperature for fabrication greater than 450 °C" is not clear. The Applicant respectfully submits that in **Paragraphs 0042** and **0044** are clear and definite in regards to layers of materials that can require fabrication at temperatures greater than 450 °C. Examples of those layers of material include the aforementioned refractory metals, a possible non-ohmic device, appropriate electrodes, contact plugs, and one or more layers of the multi-resistive state element. Therefore, one skilled in the art would understand that the aforementioned layers of material require processing at temperatures greater than 450 °C.

The Examiner also cites **MPEP 2112.01** and **MPEP 2113** as establishing processing conditions in a product claim as non-limitations in a claim. Although **MPEP 2113** addresses the procedure for examining product-by-process claims, the claims at issue in the instant Office Action are not product-by-process claims; therefore, **MPEP 2113** does not render the claims objectionable or indefinite under **35 U.S.C. §112** second paragraph.

In **MPEP 2112.01** section II, in reference to **In re Weiss, 989 F.2d 1202, 26 USPQ2d 1885 (Fed. Cir, 1993)**, for an athletic shoe with cleats that "break away at a preselected level of force", the term preselected level of force" was found to not be

ambiguous when viewed in light of the meaning ascribed to that term in the specification which defined it as "*the level of force at which breaking away will prevent injury to the wearer during athletic exertion.*" Similarly, in the present application the terms "high temperature", "stable", "not stable", or "fabrication greater than 450 °C" are not ambiguous as argued above when viewed in light of what is disclosed in the **Detailed Description** in **Paragraphs 0038 – 0044**. One skilled in the art upon reading those paragraphs will understand their meaning as used in the microelectronics art and related arts (e.g., semiconductor processing).

For all the reasons argued above, **Claims 1- 2 and Claims 4 - 48** are definite and particularly point out and distinctly claim the subject matter the Applicant regards as the invention. Therefore, the rejections of **Claims 1- 2 and Claims 4 - 48** under **35 U.S.C. §112** second paragraph ought to now be withdrawn.

b. Rejection of Claims 1- 2, 5 – 9, 24 – 28, 33 – 37, and 45 under 35 U.S.C. §102(e) (*798 - Ishii Reference*)

A prima facie case of anticipation under **35 U.S.C. §102(e)** requires every element of a rejected claim to be either explicitly or inherently disclosed in a single prior art reference. As amended herein, independent **Claims 1, 25, 33,** and **44** are not anticipated by the **798** reference (*Ishii* hereinafter) because Ishii does not disclose a two-terminal cross point memory array formed over a substrate layer that includes active circuitry having multiple layers of conductive paths. The memory cell arrays disclosed in *Ishii* require at least three terminals to access the core memory cells in the arrays. For example, see paragraph 0037 and Fig. 1, wherein source 1, drain 2, floating gate 4, and gate control line 5 are required to access the Flash memory cell. Similarly, in Fig. 10 and paragraph 0053, Ishii discloses that the memory cell requires source line 24, data line 25, and word line 29. Additionally, the SRAM memory cell arrays depicted in Figs. 8 and 9 require more than two terminals to access the unit memory cell. The same is true of the memory cell arrays depicted in Figs. 12, 13, 14, 16, 17, and 21 of *Ishii*.

Therefore, because *Ishii* does not identically disclose all of the elements of **Claims 1, 25, 33,** and **44**, it stands that those claims are not anticipated by and are patentably distinct in view of *Ishii* and the rejection of those claims under **35 U.S.C. §102(e)** ought to now be withdrawn.

Dependent Claims 2, 5 – 24, 26 – 32, 34 – 43, and **45 – 48** depend from the aforementioned independent claims and inherit all of their limitations. Therefore, those dependent claims are not anticipated by and are patentably distinct in view of *Ishii* and the rejection of those claims under **35 U.S.C. §102(e)** ought to now be withdrawn.

c. Rejection of Claims 4, 39 – 42, 44, and 46 under 35 U.S.C. §103(a) (798 and 332 References)

For a prima facie case of obviousness under **35 U.S.C. §103(a)** to stand, all claim limitations must be taught or suggested by the combination of the references and there must be a suggestion or motivation to modify or combine the references to arrive at the claimed invention. The **798** (*Ishii* hereinafter) and **332** (*Ignatiev* hereinafter) references taken individually or in combination do not teach all of the claim limitations of independent **Claims 1, 25, 33,** and **44**. First, the Examiner is incorrect in stating on page 6 of the instant Office Action that Ishii discloses "*a re-writable cross point memory*." As argue above in the **§102(e)** rejection, *Ishii* is absolutely silent and does not disclose a two-terminal cross point memory array. Moreover, the words "*a re-writable cross point memory*" are the Examiner's and not those of *Ishii* because a careful reading of Ishii will show that the words "cross point" are not set forth within the four corners of *Ishii*. Second, although though *Ishii* discloses in paragraph 0034, that MRAM can be used for the memory array, *Ishii* does not disclose that the MRAM is a cross point array or is a two-terminal cross point memory array! *Ishii* only teaches memory arrays that have more than two-terminals as argue above. Consequently, *Ishii* teaches away from the two-terminal cross point memory array of the present application.

Similarly, *Ignatiev* is silent as to forming or positioning the two-terminal memory elements in the cross point memory array above a substrate that includes active circuitry having multiple layers of conductive paths. Although the Examiner contends that the motivation to combine would be obvious to one skilled in the art because the memory array of *Ignatiev* is a much better memory device than the MRAM device of *Ishii*. The legal standard for obviousness under **§103(a)** requires that the motivation to combine references (i.e., *Ishii* and *Ignatiev*) be found in the references themselves and not through hindsight guessing by the Examiner.

Ishii discloses at least three different types of memory arrays that require more than two terminals (e.g., DRAM, SRAM, EPROM, and Flash) and further discloses that the memory array formed on the substrate is a high speed array and the memory formed over the substrate is a high density low speed memory (see paragraphs 0034 and 0035). *Ishii* teaches that the shorter interconnect distances on the substrate allow for faster access times for the memory formed on the substrate as opposed to the longer interconnect lines required to communicate with the memory array formed over the substrate. Accordingly, the combination of *Ishii* and *Ignatiev* does not lead one skilled in the art to combine the high speed, high density, two-terminal cross point array of *Ignatiev* with the three or more terminal low speed arrays of *Ishii*.

Consequently, for the reasons set forth above, **Claims 4, 39 – 42, 44, and 46** are patentably distinct and are non-obvious in view of the cited sections of *Ishii* and *Ignatiev*. Accordingly, the rejections of those claims under **35 U.S.C. §103(a)** ought to now be withdrawn.

d. Rejection of Claims 10 and 47 under 35 U.S.C. §103(a) (798, 332, and 247 References)

For at least the same reasons as argued in sections **(b)** and **(c)** above, *Ishii*, *Ignatiev*, and *Hsu* taken individually or in any combination do not teach or suggest all of the claim limitations in dependent **Claims 10** and **47**. *Hsu* does not disclose the possibility of building a cross point array directly over active circuitry and *Ignatiev* is also

silent as building a cross point array directly over active circuitry. Therefore, one skilled in the art would not be motivated to combine the teachings of *Hsu* and/or *Ignatiev* with those of *Ishii* to arrive at the two-terminal cross point memory as claimed in the present application.

Consequently, for the reasons set forth above, dependent **Claims 10** and **47** are patentably distinct and are non-obvious in view of the cited sections of *Ishii*, *Ignatiev*, and *Hsu*. Accordingly, the rejections of those claims under **35 U.S.C. §103(a)** ought to now be withdrawn.

e. Rejection of Claims 11 – 21 under 35 U.S.C. §103(a) (798, 332, 247, and 801 References)

For at least the same reasons as argued in sections **(b)**, **(c)**, and **(d)** above, the addition of *Slaughter* does not render the claims of the present application **§103(a)** obvious in view of *Ishii*, *Ignatiev*, *Hsu*, and *Slaughter* taken individually or in any combination. *Slaughter* is silent and teaches away from multi-state resistance memory elements (e.g. *Slaughter* teaches MRAM and MJT cells) and *Slaughter* is silent as to forming a two-terminal cross point memory array over a substrate with active circuitry. Therefore, one skilled in the art would not have a motivation to combine or modify the references to arrive at the claims of the present application.

Consequently, for the reasons set forth above, dependent **Claims 11 – 21** are patentably distinct and are non-obvious in view of the cited sections of *Ishii*, *Ignatiev*, *Hsu*, and *Slaughter*. Accordingly, the rejections of those claims under **35 U.S.C. §103(a)** ought to now be withdrawn.

f. **Rejection of Claims 22 – 23, 29 – 32, and 38 under 35 U.S.C. §103(a) (798 and 801 References)**

For at least the same reasons as argued in sections **(b)**, **(c)**, **(d)**, and **(e)** above, the combination of *Ishii* and *Slaughter* does not teach or suggest all the limitations of the claims as amended herein. For example, *Slaughter* is silent and teaches away from multi-state resistance memory elements (e.g. *Slaughter* teaches MRAM and MJT cells) and both *Ishii* and *Slaughter* are silent as to forming a two-terminal cross point memory array over a substrate with active circuitry.

Consequently, for the reasons set forth above, dependent **Claims 22 – 23, 29 – 32, and 38** are patentably distinct and are non-obvious in view of the cited sections of *Ishii* and *Slaughter*. Accordingly, the rejections of those claims under **35 U.S.C. §103(a)** ought to now be withdrawn.

g. **Rejection of Claims 43 and 48 under 35 U.S.C. §103(a) (798 and 944 References)**

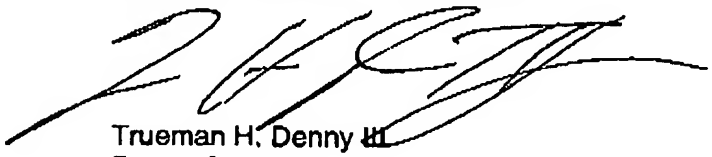
For at least the same reasons as argued in sections **(b)**, **(c)**, **(d)**, **(e)** and **(f)** above, the combination of *Ishii* and *Monsma* does not teach or suggest all the limitations of the rejected claims. *Monsma* discloses magnetic tunnel junction devices and is silent as to forming the array of magnetic tunnel junction devices over a substrate that includes active circuitry. *Ishii* is silent and teaches away from a two-terminal cross point memory array. Therefore, one skilled in the art would upon reading *Ishii* and *Monsma* would not have a motivation to combine or modify those references to arrive at the invention of **Claims 43** and **48**.

Consequently, for the reasons set forth above, dependent **Claims 43** and **48** are patentably distinct and are non-obvious in view of the cited sections of *Ishii* and *Monsma*. Accordingly, the rejections of those claims under **35 U.S.C. §103(a)** ought to now be withdrawn.

iii. CONCLUSION

Applicant now believes the present case to be in condition for allowance, and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application the undersigned can be reached at (408) 737-7200 x124.

Respectfully submitted,
Unity Semiconductor Corporation



Trueman H. Denny III
Patent Counsel
Reg. No. 44,652

250 North Wolfe Road
Sunnyvale, CA 94085-4510